UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/099,716	03/12/2002	Kenneth Okin	01.P013	1936

7590 09/28/2004

EXAMINER
CONTINO, PAUL F

ART UNIT	PAPER NUMBER
2114	

B. NOEL KIVLIN
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL,P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/099,716	OKIN, KENNETH	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Page 1 line 11 refers to "the four processors 20-50 shown" in which there is no element 50 detailed in Fig. 1 of the drawings.

Page 1 line 13 refers to "I/O interfaces 100-150" in which there are no elements 100-150 detailed in Fig. 1 of the drawings.

Page 7 line 10 discloses "HA." It is unclear what "HA" represents.

Page 8 line 14 discloses "IOC 300 with connections and responsibility for both interfaces 350 and 355" where the drawings do not depict such connections between IOC 300 and interfaces 350 and 355 as described previously in the disclosure.

Appropriate correction for all informalities is required.

Claim Objections

3. Claim 16 is objected to because of the following informalities: line 2 states "devide". Examiner treats "devide" as "device" for further consideration of the claim limitations. Appropriate correction is required.

Claims 18 and 19 are objected to because of use of parentheses. Content within parentheses is interpreted as exemplary language. Claims 18 and 19 use the language "a number $(y-x) \geq 0$," which may be interpreted as any number greater than or equal to zero, not necessarily the number "y-x".

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 10-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 10 claims a "method of manufacturing" the disclosed invention. Applicant fails to teach the method of manufacture of the "semiconductor device." The specification discloses that components of the invention are formed on a semiconductor device, however, there is no method included as to how this forming is accomplished. Claims 11-14 are rejected based upon their dependency to claim 10.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by de Corlieu et al. (U.S. Patent 4,891,810).

As in claim 1, de Corlieu et al. discloses a first number of components formed on the semiconductor device (Fig.1 #100 and 480; column 2 line 22 where the definition of computer as

stated in the prior art from is interpreted as the "semiconductor device"; definition of "computer" as stated in the Microsoft Computer Dictionary, 4th Edition, 1999: "Any device capable of processing information to produce a desired result." Both processors 100 and receivers 480 are being interpreted as "components.")

and a plurality of communication channels configured to transfer data between respective ones of the components and other elements of the system (Fig. 1 #51; column 3 lines 1-2);

wherein the semiconductor device is configured for operation in cooperation with the system using a second number of the components, the second number being less than the first number (Fig. 1 #100; column 4 lines 39-65, where it is interpreted that N is the "first number" and H is the "second number").

As in claim 2, de Corlieu et al. discloses further including a controller configured to control operations of the components (Fig. 1 #502; column 2 lines 37-40).

As in claim 3, de Corlieu et al. discloses wherein the operations include an operation of placing at least one component in a wait state (column 1 lines 23-26, column 4 lines 45-48, 56-60, and column 5 lines 9-10, where it is inherent that the "N-H" processors not being used for the computations receive a "de-activation command," thus placing them in a "wait state").

As in claim 4, de Corlieu et al. discloses the components include microprocessors (Fig. 1 #100; column 2 line 22);

and the communication channels include I/O paths connected to at least one I/O interface for the semiconductor device (Fig. 1 #480; column 2 line 67 through column 3 line 2).

As in claim 5, de Corlieu et al. discloses the components include I/O controllers (Fig. 1 #480; column 2 line 67 through column 3 line 2 and lines 10-13, where the insulation of the processor 100 from the buses 54 is interpreted as an I/O control);

and the communication channels include I/O paths connected to at least one I/O interface for the semiconductor device (Fig. 1 #480; column 2 line 67 through column 3 line 2).

As in claim 6, de Corlieu et al. discloses at least one of the components beyond the first number of components is provided as a redundant component to the first number of components (Fig. 1 #100; column 4 lines 39-48).

As in claim 7, de Corlieu et al. discloses a number z of processors formed on the semiconductor device (Fig.1 #100; column 2 line 22 and column 4 lines 39-48 where N represents "a number z");

and a plurality of I/O controllers connected to I/O interfaces for the semiconductor device and configured to control data transfer between the processors and the interfaces (Fig.1 #54, 100, and 480; column 2 line 63 through column 3 line 2, where receiving circuits 480 are interpreted as "I/O controllers" and buses 54 are interpreted as "I/O interfaces" to the supplier of the data to be stored in memory 3).

wherein the device is configured to provide a number x of operational processors for use by the processor-based system, and where the number z is greater than the number x, thereby providing a number z-x of redundant processors (Fig. 1 #100; column 4 lines 39-48 where H represents "a number x").

As in claim 8, de Corlieu et al. discloses failover logic configured to determine when one of the x processors has failed, and upon such determination to provide one of the z-x redundant processors for operation with the processor-based system (column 5 lines 53-68 and column 10 lines 1-5).

As in claim 9, de Corlieu et al. discloses logic configured to place at least one of the z-x redundant processors in a wait state (column 1 lines 23-26, column 4 lines 45-48, 56-60, and column 5 lines 9-10, where it is inherent that the "N-H" processors not being used for the computations receive a "de-activation command," thus placing them in a "wait state").

As in claim 10, de Corlieu et al. discloses a number z of components on the device (Fig.1 #100; column 2 line 22 and column 4 lines 39-48 where N represents "a number z");

control logic on the device configured to provide a number $x<z$ of operational components to operate in cooperation with the system (column 4 lines 48-52 where H represents "a number x").

As in claim 11, de Corlieu et al. discloses testing the z processors to determine a number y of functional components (column 9 line 62 through column 10 line 9 where the new N value after renumbering in the prior art is interpreted as "a number y");

and determining whether the number y is at least as great as the number x, to determine whether the semiconductor device is usable for operation with the system (column 10 lines 7-9).

As in claim 12, de Corlieu et al. discloses the components are microprocessors configured for use in a multiprocessor system (Fig. 1 #100; column 2 line 22).

As in claim 13, de Corlieu et al. discloses the components are I/O controllers configured to control I/O for the semiconductor device (Fig. 1 #480; column 2 line 67 through column 3 line 2).

As in claim 14, de Corlieu et al. discloses the step of configuring the control logic to place at least one of the components beyond the first x operational components in a wait state (column 1 lines 23-26, column 4 lines 45-48, 56-60, and column 5 lines 9-10, where it is inherent that the "N-H" processors not being used for the computations receive a "de-activation command," thus placing them in a "wait state").

As in claim 15, de Corlieu et al. discloses at least a number x (H) of components provided on a semiconductor device including a number z>x (N > H) of the components, the system including:

control logic to determine whether at least x of the components are operational, and if so, to hold any excess number of components beyond the x operational components in a backup mode (column 1 lines 23-26, column 4 lines 45-48, 56-60, and column 5 lines 9-10, where it is inherent that the "N-H" processors not being used for the computations receive a "de-activation command," thus placing them in a "backup mode").

As in claim 16, de Corlieu et al. discloses the processor-based system includes the semiconductor device, and the control logic is formed at least in part on the semiconductor device (Fig. 1 # 101 and 502; column 2 lines 20-21, column 3 line 53 through column 4 line 1, and column 5 lines 53-68, where the "control logic" is made up of the master processor 101 and the sequencer 502).

As in claim 17, de Corlieu et al. discloses the control logic is at least in part provided external to the semiconductor device (Fig. 1 #101; one skilled in the art would understand that the computer disclosed by de Corlieu et al. may be configured with sequencer 502 "on the semiconductor device" and master processor 101 "external to the semiconductor device.").

As in claim 18, de Corlieu et al. discloses the components comprise a number y of operational processors formed on the semiconductor device, where $y \geq x$, thereby providing a number $y - x \geq 0$ of backup processors for the system (column 9 line 62 through column 10 line 9 where the new N value after renumbering in the prior art is interpreted as "a number y" and column 10 line 10 where $y - x \geq 0$).

As in claim 19, de Corlieu et al. discloses the components comprise a number y of operational I/O controllers formed on the semiconductor device, where $y \geq x$, thereby providing a number $y - x \geq 0$ of backup I/O controllers for the system (column 9 line 62 through column 10 line 9 where the new N value after renumbering in the prior art is interpreted as "a number y" and column 10 line 10 where $y - x \geq 0$. It is interpreted that processor 100 of Fig. 2 as described in column 6 line 1 through column 7 line 12 control the input and output of various information, such as communicating with memory modules 3, and therefore may be considered "I/O controllers").

As in claim 20, de Corlieu et al. discloses the control logic is configured to place the excess number of components in a wait state (column 1 lines 23-26, column 4 lines 45-48, 56-60, and column 5 lines 9-10, where it is inherent that the "N-H" processors not being used for the computations receive a "de-activation command," thus placing them in a "wait state").

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (703) 605-4316 [after approximately October 15, 2004 at (571) 272-3657]. The examiner can normally be reached on Monday-Friday 7:30 am - 5:00 pm, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713 [after approximately October 15, 2004 at (571) 272-3645]. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 [after approximately October 15, 2004 at (571) 273-3657].

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PFC
September 20, 2004

SCOTT BADERMAN
PRIMARY EXAMINER